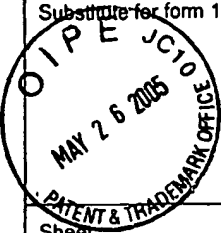
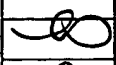

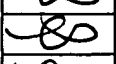

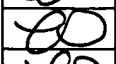
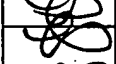



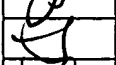





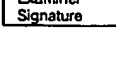
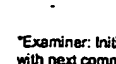
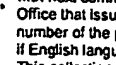
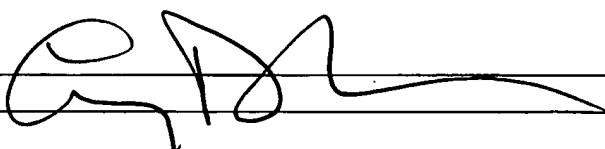


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 INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Application Number	09/312302	
			Filing Date	05/15/99	
			First Named Inventor	Adolfo M. Nemirovsky	
			Art Unit	NA	
			Examiner Name	Herewith	
Sheet	1	of	3	Attorney Docket Number	MIPS.0161-00-US

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		6105127	08-15-2000	Kozo et al	
		09/592106	filed 06-12-2000	Melvin et al.	
		09/595776	filed 06-16-2000	Musoll et al.	
		09/616385	filed 07-14-2000	Musoll et al.	
		09/629805	filed 07-31-2000	Nemirovsky et al.	
		09/312302	filed 05-15-1999	Nemirovsky et al.	
		09/273810	filed 03-22-1999	Nemirovsky et al.	
		20020062435	05-23-2002	Nemirovsky et al.	
		09/240012	filed 01-27-1999	Nemirovsky et al.	
		6356996	03-12-2002	Adams, Phillip M.	
		6260077	07-10-2001	Rangarajan et al.	
		20030084269	05-01-2003	Drysdale et al.	
		6493749	12-10-2002	Paxhia et al.	
		6430593	08-06-2002	Lindsley, Brett Louis	
		5694572	12-02-1997	Ryan, Charles P.	
		6442675	08-27-2002	Derrick et al.	
		6192384	02-20-2001	Dally et al.	
		4197579	04-08-1980	Forsman et al.	

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Application Number	09/312302
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First Named Inventor	Adolfo M. Nemirovsky
Art Unit	NA
Examiner Name	Herewith
Attorney Docket Number	MIPS.0161-00-US

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FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ² Number ⁴ Kind Code ⁵ (if known)				
BA	BA	JP10207717A2 (Translation of Relevant Parts and Abstract provided)	08-07-1998	Matsuzaki et al.		Yes
	BB	JP1011301A2 (Translation of Relevant Parts and Abstract provided)	01-16-1998	Imai et al.		Yes
	BC	JP09506752A2 (Translation of Relevant Parts and Abstract provided)	06-30-1997	Dobbins et al.		Yes
	BD	JP10124316A2 (Translation of Filing Particulars and Abstract provided)	05-15-1998	Kimura et al.		Yes
	BE	JP2103630 (Translation of Relevant Parts and Abstract Provided)	10-12-1988	Makita et al.		Yes
	BF	JP4335431 (Translation of Relevant Parts and Abstract Provided)	11-24-1992	Sakai, Noriaki		Yes
	BG	JP63254530 (Translation of Relevant Parts and Abstract Provided)	10-21-1988	Tanitsu, Eiji		Yes
	BH	JP546379 (Translation of Relevant Parts and Abstract Provided)	02-26-1993	Okazaki et al.		Yes
	BI	EP0827071A2	03-4-1998	Kimura et al.		
	BJ	WO9427216A1	11-24-1994	Keckler et al.		
BK	BK	EP0806730A2	11-12-1997	Zolnowsky, John E.		
	BL	WO0023891A1	04-27-2000	Lundstrom et al.		

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Application Number	09/312302
Filing Date	05/15/99
First Named Inventor	Adolfo M. Nemirovsky
Art Unit	NA
Examiner Name	Herewith
Attorney Docket Number	MIPS.0161-00-US

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T‡
	CA	DIEFENDORFF, KEITH, "Compaq Chooses SMT for Alpha," 12/6/99, Microprocessor Report	
	CB	DIEFENDORFF, KEITH, "WinChip 4 Thumbs Nose At ILP," Microprocessor Report, 12/7/98, Vol. 12, No. 16	
	CC	DIEFENDORFF, KEITH, "Jalapeno Powers Cyrix's M3," Microprocessor Report, 11/16/98, Vol. 12, No. 15	
	CD	SLATER, MICHAEL, "Rise Joins x86 Fray with mP6," Microprocessor Report, 11/16/98, Vol. 12, No. 15	
	CE	EGGERS ET AL., "Simultaneous Multithreading: A Platform for Next-Generation Processors," IEEE Micro, September/October 1997	
	CF	THEKKATH ET AL. The Effectiveness of Multiple Hardware Contexts. In Proceedings of the 6th International Conference on Architectural Support for Programming Languages and Operating Systems, pages 328-337, San Jose, CA, October 1994. ACM	
	CG	BECKER ET AL., "The PowerPC 601 Microprocessor," IEEE Micro, October 1993	
	CH	CUI ET AL., Parallel Replacement Mechanism for MultiThread, Advances in Parallel and Distributed Computing, 1997. Proceedings, IEEE, March 21, 1977, pp. 338-344	
	CI	MC FARLING, SCOTT. Combining Branch Predictors. WRL Technical Note TN-36. June 1993. Pages 11-12. Digital Western Research Laboratory. Palo Alto, CA, US	

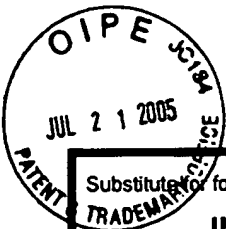
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	09/312302
				Filing Date	05/15/99
				First Named Inventor	ADOLFO M. NEMIROVSKY
				Group Art Unit	2154
				Examiner Name	LARRY DONAGHUE
Sheet	1	of	1	Attorney Docket Number	MIPS.0161-00-US

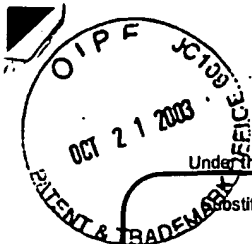
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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
AA		UNGERER ET AL. A Survey of Processors with Explicit Multithreading. ACM Computing Surveys, Vol., 35, No. 1. March 2003. Pages 29-63.	

Examiner Signature		Date Considered	05/15/99
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Application Number	09/312,302
Filing Date	05/14/1999
First Named Inventor	Mario Nemirovsky
Art Unit	2154
Examiner Name	Larry Donaghue
Attorney Docket Number	P3803

Sheet 1 of 4

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5600837 A *	02-04-1997	Artieri, Alain	
		US- 5461722 A *	10-24-1995	Goto, Tatuhiro	
		US- 5542088 A	07-30-1996	Jennings, Jr. et al.	
		US- 5748468 A	05-05-1998	Notenboom et al.	
		US- 5745778 A	04-28-1998	Alfieri, Robert	
		US- 5867725 A	02-02-1999	Fung et al.	
		US- 5309173 A *	05-03-1994	Izzi et al.	
		US- 5852726 A *	12-22-1998	Lin et al.	
		US- 5713038 A	01-27-1998	Motomura, Masato	
		US- 5812811 A *	09-22-1998	Dubey et al.	
		US- 5860017 A *	01-12-1999	Sharangpani et al.	
		US- 5784613 A	07-21-1998	Tamirsa	
		US- 5511210 A	04-23-1996	Nishikawa et al.	
		US- 6119203 A	09-12-2000	Snyder et al.	
		US- 5649144 A	07-15-1997	Gostin et al.	
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		US- 6076157 A	06-13-2000	Borkenhagen et al.	
		US- 6029228 A	02-22-2000	Cai et al.	
		US- 5561776 B1	10-01-1996	Popescu et al.	

FOREIGN PATENT DOCUMENTS

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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

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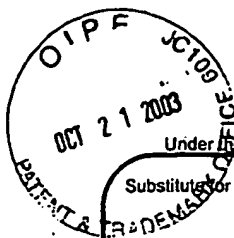
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g		* FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
b		* YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of California Santa Barbara dissertation, December 1995, Santa Barbara, US	
e		* STEERE et al., "A Feedback - Driven Proportion Allocator for Real-Rate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp 145-158, USENIX Association	
g		* YAMAMOTO et al., "Increasing Superscalar Performance Through Multistreaming", 1995	
e		* TULLSEN et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22nd Annual International Symposium on Computer Architecture, June 1995, Santa Margherita Ligure, Italy	
e		YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp 42-53, IEEE	
e		KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 Mhz", August 1998	
e		TULLSEN et al., "Supporting Fine-Grained Synchronization on a Simultaneous Multithreading Processor", 5th Annual International Symposium on Computer Architecture, January 1999	
e		NEMIROVSKY et al., "Quantitative Study of Data Caches on a Multistreamed Architecture", Workshop on Multithreaded Execution Architecture and Compilation, January 1998	
e		LI et al., "Design and Implementation of a Multiple-Instruction-Stream Multiple-Execution-Pipeline Architecture", 7th International Conference on Parallel and Distributed Computing and Systems, October 1995, Washington D.C.	

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		Filing Date			
		First Named Inventor	RECEIVED		
		Art Unit	OCT 27 2003		
		Examiner Name	Technology Center 2100		
Sheet	4	of	4	Attorney Docket Number	

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Donalson et al., "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance", 26th Hawaii Conference on Systems Sciences, 1993, pp 448-456, vol. 1	

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